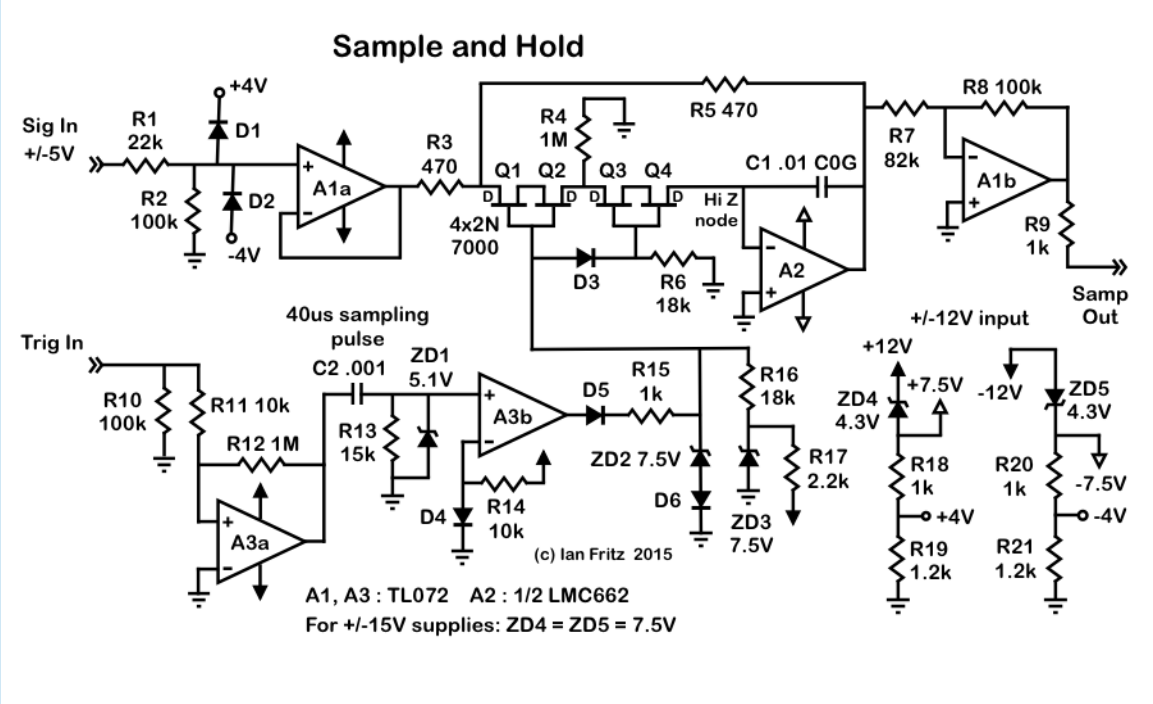
Super Sample and Hold

Here is a super S/H circuit utilizing the tiny (2 fA) input bias of the LMC662 CMOS opamp along with tandem MOSFET switches that are configured to eliminate switch leakage.



The circuit operates from +/-12 V supplies. ZD4/ZD5, R18/20 and R19/R21 provide +/- 7.5 V and +/- 4 V subregulated voltages for the CMOS opamp supply and the input clamp, respectively. These should be bypassed with capacitors to ground (not shown). Input signal levels should be in the +/- 5 V range.

A1a is an input-signal buffer, with the input levels reduced and clamped to +/- 4 V. Since currently available MOSFETs all have built-in substrate diodes, they must be used in pairs for bipolar switching appplications. Thus Q1/Q2 comprise one switch, while Q3/Q4 comprise a second one. A2 is the high-impedance buffer for the holding capacitor C1. It is configured in feedback mode to keep the input side of the capacitor at virtual ground. Realizing low leakage requires that the node marked "Hi Z node" be isolated, preferably by wiring in air, and the points where the leads enter the components need to be degreased with alcohol. A1b restores the correct polarity and level of the sampled signal.

The trigger input is squared up then differentiated by the circuitry around A3a. The sampling pulse is 40 μsec wide. A3b amplifies the pulse, which then drives the two switches. The gates of the Q1/Q2 switch swing from about -7.5 V to +8 V, providing the main sampling of the signal. The gates of Q3/Q4 swing from 0 V to +7.5 V.

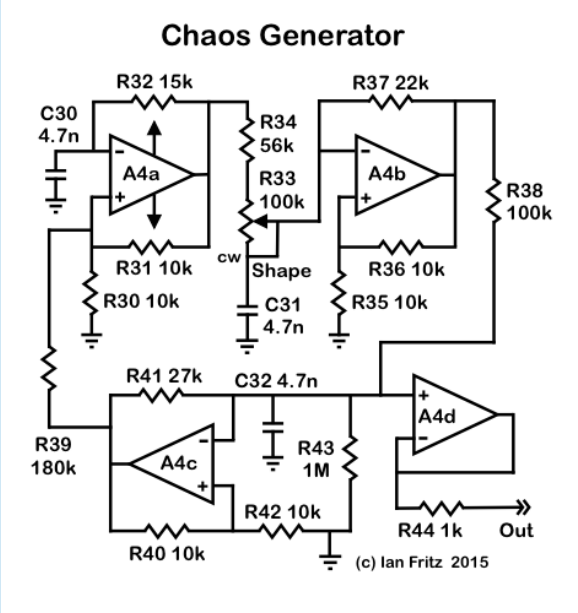
In the hold state, the second switch shunts the small leakage current from the first switch to ground via R4. Note that all the terminals of Q3/Q4 are at ground potential in the hold state, so there can be no leakage from the sampling capacitor into the switching network. This circuit configuration is similar to one described in Horowitz and Hill, "The Art of Electronics" (2nd edition, p. 393, Fig. 7.1).

Measured leakage currents with 10 nF capacitors were under 20 fA, for C0G ceramic, polypropylene, and polystyrene capacitors. For a 1 V/Oct control signal, this corresponds to under three cents of pitch drift per hour. The circuit allows sampling rates up to about 10 kHz.

Because of the four MOSFETs in the switching network, some pedestal voltage is introduced by the switching process. This amounts to about 200 mV. This offset voltage may be compensated by a current fed into the summing node of A1b if desired. Small soakage effects were observed for all three capacitor types, with C0G and polystyrene having nearly identical behavior and the smallest effect. Polypropylene capacitors were significantly worse, and are not recommended for this application.

Quasi Random/Chaotic Voltage Source

Sample and hold modules often include a random voltage source to use as a signal input. Here is a circuit with a bit of a twist on that theme.



It is a circuit that will produce a chaotic signal output and also a wide variety of multiply periodic signals. It consists of three standard single-opamp oscillators connected in a ring. The Shape control varies the signal's waveform . When tuned to a chaotic regime, the signal acts much the same as a noise source in a S/H application. When tuned into other waveforms, the sampled output is more correlated in time.